REMARKS

In the Non-Final Office Action mailed on May 5, 2004 (Paper No. 10), the Examiner rejected claims 74-81 and 100-106 under 35 U.S.C. § 112, second paragraph, as being indefinite, and rejected claims 38-42 and 57-106 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,161,160 to Niu et al. ("Niu") in view of U.S. Patent No. 5,974,483 to Ray et al. ("Ray"). In this response, Applicants amend claims 74 and 100 to more particularly point out and distinctly claim Applicants' invention. Claims 38-42 and 57-106 are pending. Further examination and review in view of the amendments and remarks below are respectfully requested.

Applicants' Techniques

Applicants' techniques are directed to multi-producer and multi-consumer accessing of a data buffer. Some of the techniques use pointers that point to a location in the data buffer to facilitate multi-producer and multi-consumer accessing of a data buffer. The pointers include an indication of a synchronization access mode to provide for unsynchronized access and for synchronized access to the data buffer. With unsynchronized access, there is no consumer and the producers can overwrite the data. With synchronized access, producers cannot overwrite the data until it is consumed. By setting the synchronization access mode to normal or sync in the pointers depending on whether it is acceptable to overwrite data, the access to the data buffer can be switched from unsynchronized to synchronized without modifying the accessing programs.

Niu

Niu discloses a random access transmit buffer and a random access receive buffer for transmission and reception of data frames between a host computer bus and a packet switched network. A memory manage unit according to Niu includes four memory management blocks for reading and writing to the buffers between the two clock domains, e.g., the host computer bus clock domain and the network clock domain. For example, the first memory management block includes a write counter for incrementing a write pointer value in response to writing data to the transmit buffer in

the host bus clock domain; the second memory management block includes a read counter for incrementing a read pointer value in response to reading data from the transmit buffer in the network clock domain; the third memory management block includes a read counter for incrementing a read pointer value in response to reading data from the receive buffer in the host bus clock domain; and the fourth memory management block includes a write counter for incrementing a write pointer value in response to writing data to the receive buffer in the network clock domain.

The memory management unit also includes a synchronization circuit that asynchronously monitors the status of the buffers, enabling the memory management blocks to read and write to the buffers between the different clock domains. The synchronization circuit includes asynchronous monitors, one for each buffer, for asynchronously monitoring the amount of stored data in their respective buffers. Each asynchronous monitor asynchronously determines the amount of data stored in its respective buffer by asynchronously comparing the write pointer and read pointer values for its buffer. The synchronization circuit and, in particular, the asynchronous monitors enable the memory management blocks to operate exclusively in their respective domains, without the necessity of synchronizing to another clock domain.

I. Rejections under 35 U.S.C. § 112, second paragraph

Claims 74-81 and 100-106 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claim 74 has been amended herein to correct the improper antecedent basis for "behavior of the accessing code." Claim 100 has been amended herein to explicitly state that "the accessing behavior depends on the synchronization access mode of the pointing means." Applicants respectfully submit that these amendments address the Examiner's concerns regarding claims 74-81 and 100-106.

II. Rejections under 35 U.S.C. § 103

All the claims stand rejected over Niu in view of Ray. Applicants respectfully traverse this rejection. All of the claims include the common feature of utilizing a synchronization access mode of a pointer, which points to a location within a buffer of

data, to be either unsynchronized or synchronized to effect a desired behavior of accessing the buffer of data. In rejecting the claims, the Examiner indicated that the full flag and status indicator flag as disclosed in Niu (col. 12, line 63 to col. 13, line 24) corresponds to the provision of setting the synchronization access mode of a pointer to effect a desired behavior of accessing the buffer of data. In particular, the Examiner stated that "the status changes from empty to full and access mode changes from write to read."

Applicants respectfully disagree. According to Niu, "[t]he synchronization circuit 60, in response to the asynchronous monitoring of the amount of data stored in the RX_SRAM 18a and the TX_SRAM 18b outputs various status indicators, flags, and status value . . . to enable a controller element to receive valid data." (col. 12, line 63 to col. 13, line 1). In Niu, a dedicated synchronization circuit monitors the amount of data stored in memory and outputs the various status indicators and flags. Moreover, as expressly stated by the Examiner, a status indicator indicates "empty" or "full," and an access mode indicates "read" or "write."

This is distinct from Applicants' feature of a pointer including a synchronization access mode, which indicates, depending on the setting of the synchronization access mode, whether the access to the buffer is unsynchronized or synchronized. First, Applicants' synchronized access mode is implemented as part of a pointer pointing to a location within the buffer of data, and not a separate synchronization circuit. Second, Applicants' synchronized access mode indicates whether the access of the buffer is unsynchronized or synchronized, and not whether the buffer is being accessed for "read" or "write." Third, Applicants' synchronized access mode does not indicate the status of the buffer as either "empty" or "full." Thus, Applicants respectfully submit that the Examiner has failed to identify how Niu either discloses, suggests or teaches utilizing a synchronization access mode of a pointer, which points to a location within a buffer of data, to be either unsynchronized or synchronized to effect a desired behavior of accessing the buffer of data. Likewise, Applicants can find in Niu no such disclosure, suggestion or teaching.

VI. Conclusion

In view of the foregoing, Applicants respectfully submit that claims 38-42 and 57-106 are allowable and ask that this application be passed to allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8000.

Respectfully submitted,
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